Listing of Claims:

(Claims 1-26 have been cancelled.)

27.(Currently Amended) A method of operating a non-volatile memory, said non-volatile memory comprising:

a plurality of word lines;

a plurality of bit lines, at least some of the plurality of bit lines being capacitively ~~inductively~~ coupled with at least a group of the plurality of word lines; and

a plurality of non-volatile memory cells individually connected to at least one of the bit lines and to one of the word lines;

wherein data are simultaneously written into at least a given number of the plurality of cells that are connected to at least one selected of said group of word lines in a programming operation that applies a first voltage to the selected word line, a second voltage to at least some of the plurality of bit lines to which said given number of cells are connected, and a reference voltage to others of said group of word lines that are not selected;

said method comprising performing said programming operation by applying a pulse of the second voltage to at least some of the plurality of bit lines to which said given number of cells are connected in a manner to avoid disturbing data stored in those of the memory cells connected to said others of said word lines that are not selected.

28.(Original) The method of claim 27, wherein a ramp rate of a leading edge of said voltage pulse is selected to control the amount of voltage that is induced thereby into said others of the word lines that are not selected.

29.(Original) The method of claim 27, wherein a number of the plurality of bit lines receiving the pulse of the second voltage is less than those which could simultaneously receive said pulse to carry out the programming operation.

30.(New) The method of claim 27, wherein a leading edge of said voltage pulse is gated by a program enable signal.

31.(New) The method of claim 28, wherein said ramp rate of a leading edge of said voltage pulse is determined by a register value.

32.(New) The method of claim 31, wherein said register value is stored in a one time programmable memory.

33.(New) The method of claim 32, the method further comprising:

setting said register value.

34.(New) The method of claim 31, wherein said register value is stored in a volatile memory, the method further comprising:

loading said register value from the non-volatile memory cells into the register.

35.(New) The method of claim 31, wherein said register value is stored in non-volatile register memory.

36.(New) The method of claim 35, wherein the memory includes a controller, the method further comprising:

programming said register value in non-volatile register memory, wherein said programming is controller by the controller.